High-Efficiency Rectifier with Wide Input Power Rage Based on a Small Capacitor in Parallel with the Diode

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***Abstract*— Based on the elimination of the input matching circuita high-efficiency microwave rectifier is presented in this work. In the proposed design, a small capacitor is in parallel with the diode, and a $\lambda_g/8$ short circuited stub is placed between the cathode of diode and ground plane. This small capacitor can modify the real part of the diode impedance, and then the $\lambda_g/8$ cancels the yield capacitive impedance. Meanwhile, this $\lambda_g/8$ short circuited stub presents a high reactance at the second harmonic. The fabricated rectifier has a maximum RF-DC conversion efficiency (PCE) of 86.7% at 24.8 dBm input power. The measured efficiency remains above 70% with the input power from 8.2 to 25 dBm and the operating frequency from 1.5 to 2.2 GHz.**

***Keywords*— High efficiency, harmonic termination, wireless power transmission, wide input power range**

I. Introduction

To improve the overall efficiency of a wireless power transfer system, the RF-DC conversion efficiency (PCE) of a rectifier which converts microwave power to DC power, should be as high as possible. Recently, harmonic terminations provide an effective way to boost the conversion efficiency of a rectifier. In a Class-C diode rectifier [1], the short-circuit terminations at the second and third harmonics are designed to improve the PCE, which demonstrates a peak PCE of 72.8% at 8 dBm input power. On top of this, with a Class-F harmonic termination, the diode current and voltage form could be shaped to half sine wave and square respectively, and thus the overlap of current and voltage is minimized, which leads to an improved conversion efficiency. Some reported high efficiency Class-F rectifiers have PCEs of 80.4% at 900 MHz [2], 77.9% at 2.45 GHz [3] and 40.3% at 24 GHz [4] respectively. However, the harmonic terminations in previous literature are sensitive to parasitic parameter because the parasitic capacitance or inductance and junction capacitance are directly connected to the harmonic termination, and then the open circuit condition may not be satisfied. To avoid the insertion loss of the input low-pass filter, we propose a novel rectifier which has removed the input low-pass filter. At the same time, the proposed rectifier employs a second harmonic terminations to boost the conversion efficiency. As a result, the harmonic components of the proposed rectifier are low enough that the input low-pass filter is not a necessity. Besides, we utilize a lumped DC-pass filter to choke the RF signal before the DC load. Finally, the fabricated rectifier has a very compact size when compared to a DC-pass filter using a $\lambda/4$ transmission line terminated with a capacitor.

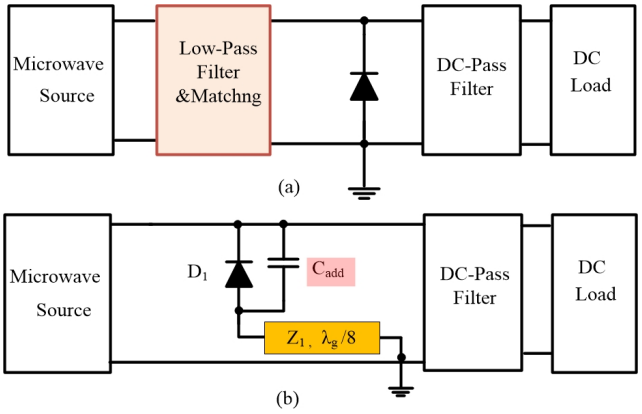

Fig. 1. (a) Conventional rectifier with a input low-pass filter. (b) The proposed rectifier has a small capacitor C_{add} which is in parallel with the diode.

II. Principle And Design Method

A. Principle

A conventional diode rectifier is shown in Fig. 1(a) where the input low-pass filter and the DC-pass filter are applied to recycle the harmonic power. To prevent the leakage of the harmonic power, the conventional rectifier needs a high performance DC-pass filter to block the harmonics.

As the input low-pass filter brings a certain insertion loss, we propose a novel topology which has the input matching circuit removed. The conceptual diagram of the proposed rectifier is shown in Fig. 1(b). Observed that an additional chip capacitor C_{add} is in parallel with the diode, and a $\lambda_g/8$ short circuited stub with a characteristic impedance Z_1 is in series with the diode. Here, the λ_g is the guided wavelength of in the transmission line at the center frequency. The C_{add} can modify the real part of the input impedance of rectifying diode(D_1), and the $\lambda_g/8$ short circuited stub will function as diode impedance matching and harmonic termination at the same time.

B. Theoretical Analysis and Simulation

At given input power and DC load, the input impedance of a Schottky diode can be modeled by a resistor R_e in parallel with a capacitor C_e. To simplify the mathematic analysis, the package parameters of diode are ignored in the equivalent circuit. Thus, the input impedance of a diode can be written as

$$Z_D = \frac{R_e}{1+(R_eC_e\omega)^2} - j\frac{R_e^2C_e\omega}{1+(R_eC_e\omega)^2} \qquad (1)$$

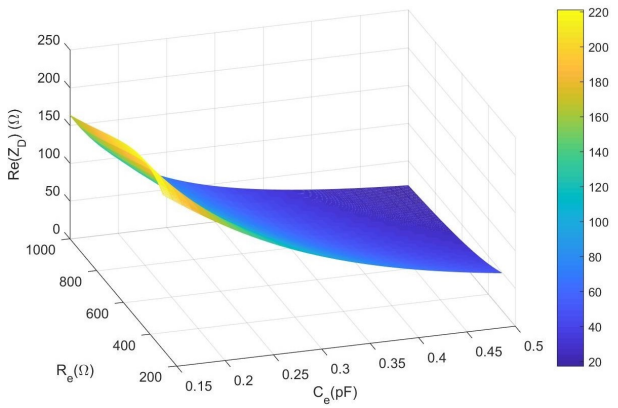

Fig. 2. The real part of the diode impedance Re(Z_D) is reduced by the increasing of junction capacitance C_e, the frequency is set to 2.4 GHz.

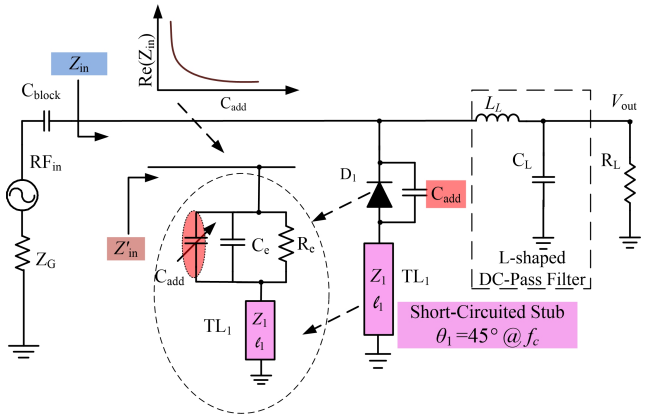

Fig. 3. The schematic the proposed rectifier, a small capacitor C_{add} is in parallel with the diode D_1.

As to first term of the (1) at a single frequency point, for arbitrary junction resistance R_e the real part of the diode impedance Re(Z_D) decreases as the C_e increases, which is plotted in the Fig. 2. Observed that, notwithstanding the variation of R_e, the Re(Z_D) decreases continuously as the C_e increases from 0.1 pF to 0.5 pF.

With the above discussion, as shown in Fig. 3, the proposed rectifier has the input matching circuit removed, and a small capacitor C_{add} functions parallel to rectifying diode D_1 to tune the real part of the diode impedance when necessary. The short circuited stub TL_1 will compensate the yield imaginary part of the input impedance looking into the rectifier. As the input impedance of the DC-pass filter is infinity (∞) at all frequencies, the input impedance of the linear equivalent circuit shown in Fig. 3 can be expressed as

$$Z'_{\text{in}} = [(C_e + C_{\text{add}}) \parallel R_e] + jZ_1 \tan(\beta\ell_1) \tag{2}$$

Let $C_{\text{sum}} = C_e + C_{\text{add}}$, as $\beta\ell_1 = \pi/4$, and thus (2) can be rewritten as (3) where the angular velocity $\omega = 2\pi f_c$.

$$Z'_{in} = \frac{R_e}{1 + (R_e\omega C_{sum})^2} - j * \frac{{R_e}^2\omega C_{sum}}{1 + (R_e\omega C_{sum})^2} + jZ_1 \tag{3}$$

As indicated in equation (3), the real part of input impedance Re(Z'_{in}) can be reduced by increasing C_{sum} through a large C_{add}.

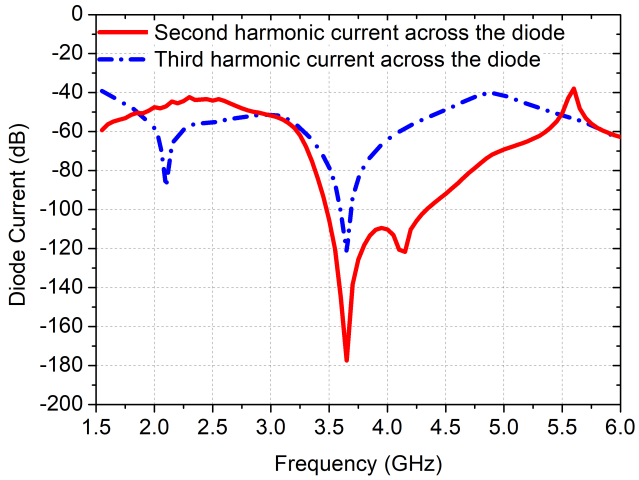

Fig. 4. Simulated diode current spectra in dB over 1.5-6 GHz.

The input matching of the proposed rectifier requires that Re(Z'_{in})=50Ω and Im(Z'_{in})=0, which gives two equations for the C_{add} and Z_1 (characteristic impedance of TL_1).

$$C_{add} = \frac{\sqrt{R_e/50 - 1}}{R_e\omega_c} - C_e \tag{4}$$

$$Z_1 = \frac{{R_e}^2\omega_c C_{sum}}{1 + (R_e\omega_c C_{sum})^2} \tag{5}$$

Consider the electrical length of the short circuited stub TL_1 which shown in Fig. 3. The input impedance of the $\lambda_g/8$ short circuited stub at different frequencies short circuit stub at different frequencies (DC, f_c, $2f_c$ and $3f_c$) are described by (6) below [5]

$$Z_{\lambda g/8} = jZ_1 \tan(\frac{\pi}{4}\frac{f}{f_c}) = \begin{cases} 0 & f = 0 \\ jZ_1 & f = f_c \\ \infty & f = 2f_c \\ -jZ_1 & f = 3f_c \end{cases} \tag{6}$$

The (6) implies that the $\lambda_g/8$ serves as a second harmonic termination at the same time, because the input impedance of the short circuited $\lambda_g/8$ is ∞ at $2f_c$. As a result, the second harmonic currents flowing through the diode can be attenuated significantly.

The proposed rectifier is simulated by using both the harmonic balance method and large signal S-parameter (LSSP) in Advance design system (ADS, Keysight). The SPICE model of HSMS-282 diode is provided by ADS program. The C_{add} used in the nonlinear simulation is 0.2 pF. The short circuited stub TL_1 has a physical length of 12 mm, for which the electrical length is around $\lambda_g/8$ at 1.8 GHz.

Fig. 4 shows the corresponding spectra of the diode current versus the operating frequency. With the sweep of the RF frequency, it can be clearly observed that the second harmonic current has been blocked at around 3.6 GHz. Around 5.4 GHz, the third harmonic current is about 10 dB larger than the average value. The high impedance second harmonic termination and relatively low impedance third harmonic termination are achieved by the $\lambda_g/8$ short circuited stub.

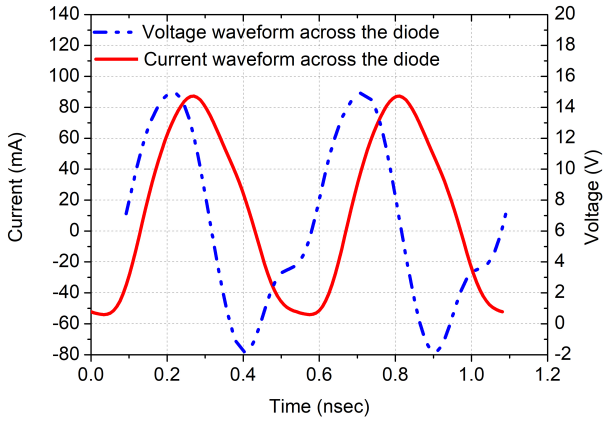

Fig. 5. Simulated time-domain current and voltage waveform on the rectifying diode D_1.

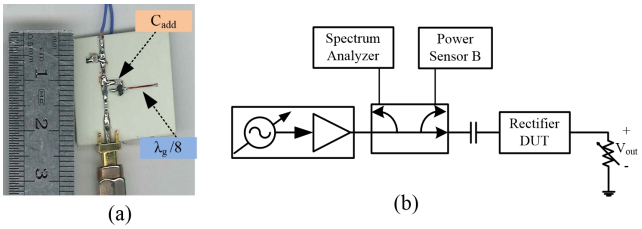

Fig. 6. (a) A photograph of the fabricated rectifier. (b) The measurement setup for the PCE and the input harmonics levels.

Besides, the simulated voltage and current waveforms across the diode at 20 dBm input power are shown in Fig. 5 where the shape of diode current closely resembles to a sine wave. The proposed rectifier can be considered as an inverse class-C rectifier.

III. Implementation and Experimental Results

A photograph of the fabricated rectifier is shown in Fig. 6, it has been fabricated in accordance with the schematic shown in Fig. 3. The substrate used for this design is Rogers4350B, and the fabricated rectifier has a very compact dimension of 25×30 mm. The measurement setup is also shown in Fig. 6. In the experiment, the proposed rectifier was measured in terms of PCE versus the input power and operating frequency. The measurements are compared with the simulation results in Fig. 7 and Fig. 8.

At first, the proposed rectifier was measured under a frequency sweep with a fixed 400 Ω load and 20 dBm input power. The measured and simulated PCE are depicted in Fig. 7, and the input $|S_{11}|$ is also included. As shown, PCE of higher than 70% can be obtained from 1.5 GHz to 2.02 GHz. Due to the fabrication tolerance, there exists a slight frequency shift between the simulation and measurement, but the results still agree with each other.

Fig. 8 depicts both the simulated and measured PCE versus input power with a constant 400 Ω load at 1.8 GHz. The measured PCE goes over 70% at 8.2 dBm and remains greater than 80% when input power exceeds 13.2 dBm. It can be seen that the 86.7% peak efficiency occurs at 24.8 dBm. The measured PCE maintains more than 80% from 13.2 dBm to

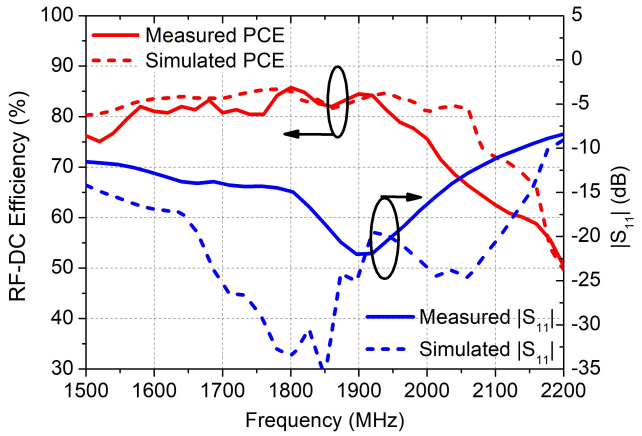

Fig. 7. The PCE and the input $|S_{11}|$ versus frequency at 20 dBm input power and 400 Ω load.

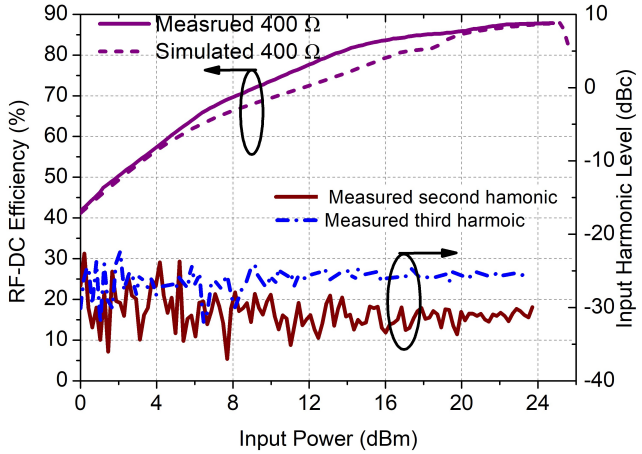

Fig. 8. The PCE and input $|S_{11}|$ versus frequency at 20 dBm input power and 400 Ω load.

25 dBm, which is a relatively wide input power range. The measurement results agree well with the simulation. Fig. 8 also plots the input harmonic levels measured by a directional coupler, both second and third harmonic levels at the input port are below -20 dBc.

In Table I, the performance of this work is compared with several recently published rectifiers. Direct comparison is made and the proposed rectifier exhibits the widest dynamic input power range and the highest fractional bandwidth. As indicated, the 16.8 dB input power range for PCE of higher than 70% is very impressive. Meanwhile, only one diode is used and the physical size is 25×30 mm which is the smallest among the four structures.

IV. Conclusion

A novel matching method for high-efficiency, wide input range rectifier has been presented. The proposed topology has the input matching network removed to avoid insertion loss. Meanwhile, the proposed design maximizes the RF-DC efficiency by the implementation of a second harmonic termination. Theoretical analysis of the proposed topology has been carried out and the circuit has been implemented. Compared to other reported rectifiers with a wide input power

Table 1. Comparison with the Prior Rectifiers

Reference		[6]	[7]	[8]	This work
P.R. for PCE>70%		8 dB	N.A.	7 dB	16.8 dB
P.R. for PCE>50%		17.3 dB	N.A	18 dB	24 dB
Peak Eff.	Eff.	80.8%	81%	77%	86.7%
	Power	17.2 dBm	10 dBm	17.2 dBm	20.5 dBm
	Fre.	2.45 GHz	1.62 GHz	1.8 GHz	1.8 GHz
Rectifier Element		HSMS286	HSMS286	HSMS282	HSMS282
Number of diode		4	2	1	1
Dimension (mm^2)		N.A	70×20	35×15	25×30

range, the proposed topology has shown the widest input range for PCE greater than 70%.

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REFERENCES

[1] M. Roberg, T. Reveyrand, I. Ramos, E. A. Falkenstein, and Z. Popovic, High-Efficiency Harmonically Terminated Diode and Transistor Rectifiers, *IEEE Trans. Microw. Theory Tech.*, vol. 60, no. 12, pp. 40434052, Dec. 2012.

[2] J. Guo and X. Zhu, Class F rectifier RF-DC conversion efficiency analysis, in *2013 IEEE MTT-S International Microwave Symposium Digest (MTT)*, 2013, pp. 14.

[3] A. Noda and H. Shinoda, Compact class-F RF-DC converter with antisymmetric dual-diode configuration, in *Microwave Symposium Digest (MTT)*, 2012 IEEE MTT-S International, 2012, pp. 13.

[4] K. Hatano, N. Shinohara, T. Mitani, T. Seki, and M. Kawashima, Development of improved 24GHz-band class-F load rectennas, in *Microwave Workshop Series on Innovative Wireless Power Transmission: Technologies, Systems, and Applications (IMWS)*, 2012 IEEE MTT-S International, 2012, pp. 163166.

[5] D. M. Pozar, Microwave engineering. *John Wiley Sons*, 2009.

[6] X. Y. Zhang, Z. Du, and Q. Xue, High-Efficiency Broadband Rectifier With Wide Ranges of Input Power and Output Load Based on Branch-Line Coupler, *IEEE Trans. Circuits Syst*. Regul. Pap., vol. 64, no. 3, pp. 731739, Mar. 2017.

[7] H. Sakaki and K. Nishikawa, Broadband rectifier design based on quality factor of input matching circuit, in *2014 Asia-Pacific Microwave Conference*, 2014, pp. 12051207.

[8] D. Wang, X. A. Nghiem, and R. Negra, Design of a 57% bandwidth microwave rectifier for powering application, in *2014 IEEE Wireless Power Transfer Conference*, 2014, pp. 6871.